CLAIMS

We claim:

1. An universal testing module, capable of connecting to a computer having communication ports to be tested and forming communication paths through said ports, for testing the condition of each pin of a parallel port and a serial port of said communication ports, at least comprising:

a logic control unit, having at least a pair of input/output ports for communicating with said parallel port;

a memory unit for storing instructions for controlling said logic control unit and said computer and for temporary exchange of data; and an universal asynchronous receiver/transmitter; and

a voltage converter for voltage interchange of RS-232 and TTL and enabling said logic control unit to communicate with said computer through said serial port and executing said testing.

2. An universal testing module according to claim 1 wherein said memory unit comprises:

an electrically erasable programmable read-only memory for storing machine code instructions for testing said communication port; and

a random-access memory for temporary exchange of data.

3. An universal testing module according to claim 1 wherein said memory unit is located outside said logic control unit.

4. An universal testing module according to claim 1 further comprising a clock circuit for providing time signals, and a reset circuit.

5. A method for detecting electrical condition of communication ports of a computer, including all pins of parallel and serial ports, comprising steps of:

1) providing a testing module connectable through pins of said parallel or serial ports and communicating with said computer;

2) initializing registers which are corresponding to said pins to a predetermined value;

3) transferring a predetermined data between said communication ports and said computer, and recording received data into said registers; and

4) comparing said received data with said predetermined data and judging open, short and normal conditions of said pins.

6. A method for detecting electrical condition of communication ports according to claim 5 wherein said step 3) further comprises steps of:

a) outputting certain data from said computer, and reading status at said testing module via said parallel and serial ports by a walk 0' and a walk 1' logic test separately, and recording a first testing result; and

b) outputting certain data from said testing module, and reading status of said computer via said parallel and the serial ports by a walk 0' and a walk 1' logic test separately, and recording a second testing result.

7. A method for detecting electrical condition of communication ports of a computer, including all pins of parallel and serial ports, by using a testing module communicating via said communication ports with said computer, comprising steps of:

a) initializing corresponding registers of said pins to a certain value;

b) checking if communications between said testing module and said communication ports succeed, if yes, jumps to step d), or proceeds to step c);

c) assuring that pins RD, TD and GND of said serial port fail, then jumps to step g);

d) outputting certain data from said computer, and reading status at said testing module via said parallel and serial ports by a walk 0' and a walk 1' logic test separately, and recording a first testing result;

e) outputting certain data from said testing module, and reading status of said computer via said parallel and serial ports by a walk 0' and a walk 1' logic test separately, and recording a second testing result;

f) outputting said first and the second testing results; and

g) finishing said test.

8. A method for detecting electrical condition of communication ports according to claim 7 wherein sequence of said step d) and said step e) are exchanged.

9. A method for detecting electrical condition of communication ports according to claim 7 wherein said step d) further comprises steps of:

d1) setting an output pin PINx at said computer side with logic value "low", and other pins with value 'high";

d2) reading logic values of pins at said testing module side, and recording values in said registers corresponding to said pins as a data record;

d3) checking if only value of said PINx is "low", if yes, jumps to step d5), or proceeds to step d4);

d4) if said PINx is high, said PINx is open; if any other pin PINy excepting from said PINx is also low, said PINy is short with said PINx;

d5) setting an output pin PINx at said computer side with logic value "high", and other pins with value "low";

d6) reading logic values of pins at said testing module side, and recording values in said registers corresponding to said pins as a data record;

d7) checking if only value of said PINx is "high", if yes, jumps to step d9), or proceeds to step d8);

d8) if said PINx is low, said PINx is open; if any other pin PINy excepting from said PINx is also high, said PINy is short with said PINx; Jumps to step d10);

d9) assuring said PINx is normal;

d10) checking if all output pins at said computer side are tested, if yes, jumps to step e), or returns to step d1) for testing next output pin.

10. A method for detecting electrical condition of communication ports according to claim 7 wherein said step e) further comprises steps of:

e1) setting an output pin PINx at said testing module side with logic value "low", and other pins with value "high";

e2) reading logic values of pins at said computer side, and recording values in said registers corresponding to said pins as a data record;

e3) checking if only value of said PINx is "low", if yes, jumps to step e5), or proceeds to step e4);

e4) if said PINx is high, said PINx is open; if any other pin PINy excepting from said PINx is also low, said PINy is short with said PINx;

e5) setting an output pin PINx at said testing module side with logic value "high", and other pins with value "low";

e6) reading logic values of pins at said computer side, and recording values in said registers corresponding to said pins as a data record;

e7) checking if only value of said PINx is "high", if yes, jumps to step e9), or proceeds to step e8);

e8) if said PINx is low, said PINx is open; if any other pin PINy excepting from said PINx is also high, said PINy is short with said PINx; jumps to step e10);

e9) assuring that PINx is normal;

e10) checking if all output pins at said testing module are tested, if yes, jumps to step f), or returns to step e1) for testing next pin.

11. A testing module for testing open condition of pins of a parallel port of a computer by connecting to pins of said parallel port, comprising:

at least a selection line connecting to output pins of said parallel port;

at least a data line connecting to output pins of said parallel port; and

at least an output line connecting to input pins of said parallel port;

whereby a certain signal output from said output line to said selection line makes signal of a certain data line transfer to said parallel port via said output line, and judge if said parallel port is normal by comparing an operating logic value with a received value.

12. A testing module for testing open condition of pins of a parallel port according to claim 11 wherein said testing module is composed of several logic circuit cells.

13. A testing module for testing open condition of pins of a parallel port according to claim 12 wherein said logic circuit cells are selectors.

14. A method for testing open condition of pins of a parallel port of a computer by connecting a testing module to pins of said parallel port, comprising steps of:

1) providing a selector composed of at least a selection line, at least a data line and at least an output line;

2) outputting a certain signal from said output line to said selection line and said data line, and making said selector transferring signal of a certain data line to said output line as a received value, and

3) judging if said parallel port is normal by comparing an operating logic value with said received value.

15. A method for testing open condition of pins of a parallel port according to claim 14 wherein said selector is composed of several logic circuit cells.

16. A method for testing open condition of pins of a parallel port according to claim 14 wherein said judgment in step 3) is made that said parallel port is normal when

said operating logic value is same with said received value; and abnormal when said operating logic value is different from said received value.

17. A logic control unit for testing open condition of a parallel port of a computer, comprising:

a first gate having a first data end, a first output end and a first control end;

a second gate having a second data end, a second output end and a second control end;

a flip-flop connecting to said second control end;

a first pin connecting to said first data end;

a second pin connecting to said first control end and said flip-flop;

a third pin connecting to said second data end;

a fourth pin connecting to said first output end and said second output end.

18. A logic control unit according to claim 17 wherein said flip-flop is changed to connect to said first control end.

19. A logic control unit according to claim 17 wherein said first, second and third pin are selectively connected with a pull up resistor for stabilizing voltage when any of said pins is open.

20. A logic control unit according to claim 17 wherein said first, second and third pin are selectively connected with a pull down resistor for stabilizing voltage when any of said pins is open.

21. **A cable multi-tap substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3 to 6 of the accompanying drawings.**

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